WL-TR-89-80

PROTON RESPONSES ON MOS ELECTRONICS OPERATING AT CRYOGENIC TEMPERATURES

R. W. Tallon
A. H. Hoffland
W. T. Kemp
J. W. Brouse

January 1990

Final Report

Weapons Laboratory
Air Force Systems Command
Kirtland Air Force Base, NM 87117-6008

REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-0188

1. AGENCY USE ONLY (Leave blank)	2. REPORT DATE	3. REPORT TYPE AND DATES COVERED
	January 1990	Final Report - Jun 87-Dec 89

4. TITLE AND SUBTITLE
PROTON RESPONSES ON MOS ELECTRONICS OPERATING AT CRYOGENIC TEMPERATURES

5. FUNDING NUMBERS
PE: 601101F
PR: ILIR
TA: 87
WU: 20

6. AUTHOR(S)
Tallon, R. W.; Hoffland, A. H.; Kemp, W. T.; Brouse, J. W.

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
Weapons Laboratory
Kirtland AFB, NM 87117-6008

8. PERFORMING ORGANIZATION REPORT NUMBER
WL-TR-89-80

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)

10. SPONSORING/MONITORING AGENCY REPORT NUMBER

11. SUPPLEMENTARY NOTES

12a. DISTRIBUTION/AVAILABILITY STATEMENT
Approved for public release; distribution unlimited.

12b. DISTRIBUTION CODE

13. ABSTRACT (Maximum 200 words)

This report presents proton radiation damage data demonstrating that Metal-Oxide-Semiconductor (MOS) electronics (P-Channel or N-Channel), operated under applied negative gate biases and irradiated by 10 MeV protons, will suffer greater radiation damage per dose at cryogenic temperatures than at room temperatures. This was true for both radiation hardened and nonradiation hardened MOS structures. However, the data also showed that this was not true for all MOS devices operating under positive gate biases. Nonradiation hardened MOS units operating under positive gate biases and bombarded by the 10 MeV protons suffered less radiation damage per dose at cold temperatures than at room temperatures. Radiation hardened MOS units, tolerant to 100 Krad(Si) and irradiated by 10 MeV protons under positive gate biases, suffered radiation damages that were approximately equal at both the cold and room temperatures. Final data showed if irradiated cold temperature MOS devices were allowed to heat to ≈-123°C or warmer, the radiation damage within the devices would anneal rapidly.

14. SUBJECT TERMS		15. NUMBER OF PAGES
Cryogenic Temperatures	Test Methods	36
Bulk Silicon	Radiation Effects	16. PRICE CODE
Protons		

17. SECURITY CLASSIFICATION OF REPORT	18. SECURITY CLASSIFICATION OF THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
Unclassified	Unclassified	Unclassified	UL

GENERAL INSTRUCTIONS FOR COMPLETING SF 298

The Report Documentation Page (RDP) is used in announcing and cataloging reports. It is important that this information be consistent with the rest of the report, particularly the cover and title page. Instructions for filling in each block of the form follow. It is important to ***stay within the lines*** to meet ***optical scanning requirements***.

Block 1. Agency Use Only *(Leave blank)*.

Block 2. Report Date. Full publication date including day, month, and year, if available (e.g. 1 Jan 88). Must cite at least the year.

Block 3. Type of Report and Dates Covered. State whether report is interim, final, etc. If applicable, enter inclusive report dates (e.g. 10 Jun 87 - 30 Jun 88).

Block 4. Title and Subtitle. A title is taken from the part of the report that provides the most meaningful and complete information. When a report is prepared in more than one volume, repeat the primary title, add volume number, and include subtitle for the specific volume. On classified documents enter the title classification in parentheses.

Block 5. Funding Numbers. To include contract and grant numbers; may include program element number(s), project number(s), task number(s), and work unit number(s). Use the following labels:

C	- Contract	PR	- Project
G	- Grant	TA	- Task
PE	- Program Element	WU	- Work Unit Accession No.

Block 6. Author(s). Name(s) of person(s) responsible for writing the report, performing the research, or credited with the content of the report. If editor or compiler, this should follow the name(s).

Block 7. Performing Organization Name(s) and Address(es). Self-explanatory.

Block 8. Performing Organization Report Number. Enter the unique alphanumeric report number(s) assigned by the organization performing the report.

Block 9. Sponsoring/Monitoring Agency Name(s) and Address(es). Self-explanatory.

Block 10. Sponsoring/Monitoring Agency Report Number. *(If known)*

Block 11. Supplementary Notes. Enter information not included elsewhere such as: Prepared in cooperation with...; Trans. of...; To be published in.... When a report is revised, include a statement whether the new report supersedes or supplements the older report.

Block 12a. Distribution/Availability Statement. Denotes public availability or limitations. Cite any availability to the public. Enter additional limitations or special markings in all capitals (e.g. NOFORN, REL, ITAR).

- DOD - See DoDD 5230.24, "Distribution Statements on Technical Documents."
- DOE - See authorities.
- NASA - See Handbook NHB 2200.2.
- NTIS - Leave blank.

Block 12b. Distribution Code.

- DOD - Leave blank.
- DOE - Enter DOE distribution categories from the Standard Distribution for Unclassified Scientific and Technical Reports.
- NASA - Leave blank.
- NTIS - Leave blank.

Block 13. Abstract. Include a brief *(Maximum 200 words)* factual summary of the most significant information contained in the report.

Block 14. Subject Terms. Keywords or phrases identifying major subjects in the report.

Block 15. Number of Pages. Enter the total number of pages.

Block 16. Price Code. Enter appropriate price code *(NTIS only)*.

Blocks 17. - 19. Security Classifications. Self-explanatory. Enter U.S. Security Classification in accordance with U.S. Security Regulations (i.e., UNCLASSIFIED). If form contains classified information, stamp classification on the top and bottom of the page.

Block 20. Limitation of Abstract. This block must be completed to assign a limitation to the abstract. Enter either UL (unlimited) or SAR (same as report). An entry in this block is necessary if the abstract is to be limited. If blank, the abstract is assumed to be unlimited.

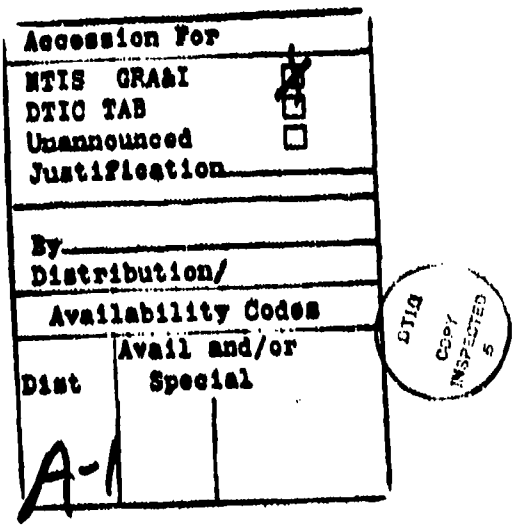
SUMMARY

This report presents and discusses proton response data taken on Metal-Oxide-Semiconductor (MOS) electronics operating at room and cryogenic temperatures. The data were collected by Weapons Laboratory (WL) personnel while performing radiation tests at the Los Alamos National Laboratory (LANL) Tandem Van de Graaff Accelerator. The objectives of this work were (1) to measure 10 MeV proton responses in MOS electronics operating at cryogenic temperatures, and (2) determine if these responses can be correlated with cold temperature irradiations from Cobalt-60 (Co^{60}) gamma rays and high energy electrons. The overall results showed that the primary radiation damage mechanism from 10 MeV protons bombarding cryogenically operated MOS electronics is similar to that of Co^{60} gamma rays and energetic electrons. That is, at cold temperatures, the radiation-induced "holes" generated in MOS gate oxides by the 10 MeV protons are "frozen in place" near the point of creation. The result is a large hole population that has escaped recombination and is distributed throughout the oxide (away from the interfaces). The outcome is that for equal amounts of total ionizing dose absorbed, the radiation damage produced in biased MOS structures at cryogenic temperatures is not equal to that caused by similar irradiations at room temperatures. Results from this work showed that all the MOS samples (radiation hardened and nonhardened), operating under negative gate biases and irradiated by the protons, suffered greater radiation damage per

dose at the selected cryogenic temperatures (-170°C to -177°C) than at room temperatures. The nonradiation hardened MOS transistors bombarded by the 10 MeV protons, under positive gate biases, suffered less radiation damage per dose at the cold temperatures than at the room temperatures. Radiation hardened MOS structures, tolerant to 100 Krad(Si) and irradiated by protons under positive biases, suffered radiation damages that were approximately equal at both the cold and room temperatures.

PREFACE

The authors wish to acknowledge the outstanding technical support provided by the test personnel at the Los Alamos National Laboratory's (LANL) Tandem Van de Graaff Accelerator. We would also like to give a special thanks to Larry Rowton of LANL for his guidance and technical expertise in the successful construction of the cryogenic test chamber.



CONTENTS

FIGURES

1.0 INTRODUCTION

Past research (Refs. 1 through 5) has shown that when Metal-Oxide-Semiconductor (MOS) transistors were irradiated with Cobalt-60 (Co^{60}) gamma rays or energetic electrons, the ionizing radiation damage produced in the devices was not only influenced by an applied electrical field across the gate oxide, but also affected by the operating temperature of the samples. The investigations showed that when a MOS device was cooled to temperatures below 150 K (-123°C) and irradiated with ionizing radiation, the resulting damage was noticeably different from the radiation damage at room temperatures (+20°C to +27°C). Research also showed that if "radiation-hardened" MOS devices were irradiated at the temperature of liquid nitrogen (-197°C), the radiation damage at the cold temperature was significantly greater than the radiation damage at room temperature.

The model that best explains this phenomenon is based on the knowledge that (1) the mobility of "holes" generated in a gate oxide layer of a MOS transistor by ionizing radiation is significantly lower than the mobility of a generated electron, and (2) the mobilities of both the created holes and electrons in the oxide decrease as the temperature drops.

For a MOS device under room temperature conditions, radiation induced electron-hole pairs will be generated in the gate oxide and will separate under the influence of an applied electrical field. Because of their high mobility, the electrons will be

rapidly swept out of the oxide. The surviving holes (with low mobility) will be transported slowly and accumulate near one of the two oxide interfaces. If a negative electrical field is applied across the oxide, as it would be for an enhancement mode P-Channel MOS (PMOS) transistor, the holes will accumulate near the metal-oxide-interface. If a positive field is applied, as it would be for an enhancement mode N-Channel MOS (NMOS) device, the holes will collect near the oxide-silicon-interface. The result (in either case) will be a "flatband" or gate threshold voltage (Vth) shift that is proportional to the total ionizing dose received. Because they are closer to the bulk silicon, the holes collected at the oxide-silicon-interface by the positive electrical field will have a greater adverse effect on the channel current than the holes accumulated at the metal-oxide-interface by the negative electrical field. For this reason, an NMOS transistor should experience a greater radiation damage than a "complementary" PMOS transistor receiving a similar radiation dose at room temperature.

When a MOS transistor is operated at cryogenic temperatures with low electrical fields, the holes generated in the gate oxide by ionizing radiation are essentially immobile and remain trapped at the point of creation. In contrast, the generated electrons, which are still mobile in the oxide (even at temperatures as low as 4 K), are swept out of the gate insulator. The remaining holes, which are large in number (because of low recombination), are assumed to be trapped uniformly throughout the oxide. This

large number of "frozen-in" holes often results in radiation damage to the MOS device that is more severe than the damage observed at room-temperatures.

The cold-temperature model was derived from data recorded for Co^{60} gamma rays and high energy electrons. Since silicon MOS electronics are now being considered for cold temperature applications in outer space, it is important to determine if this model is valid for other types of radiations occurring in the natural space environment. One of these ionizing radiations that has not been thoroughly studied/researched at cryogenic temperatures is high energy protons. Unlike Co^{60} and electron-beam irradiations, which distribute electron-hole pairs in an isotropic manner throughout the gate oxide, bombarding protons distribute their electron-hole pairs in ionized regions localized around the tracks of the incident particles. Because the model is based on the assumption that the frozen-in holes are trapped uniformly throughout the oxide, the validity of the model for heavy particles that generate dense ionized tracks (such as protons) was in question.

To address this question, the Weapons Laboratory (WL) conducted an in-house effort to determine if the ionizing radiation damage mechanisms in MOS type electronics, being bombarded by protons at cryogenic temperatures, can be correlated with Co^{60} results. This report presents the findings of this work.

2.0 EXPERIMENT PROCEDURES

The objective of this investigation was twofold: (1) to measure the effects of ionizing radiation on MOS type electronics irradiated by protons at cryogenic temperatures, and (2) to decide if these cold temperature proton responses correlate with cold temperature Co^{60} and high energy electron irradiations.

To accomplish this task, four different MOS device types had their protective covers removed and irradiated at room and at cold temperatures with 10 MeV protons at 0 deg angles of incidence. Seconds after exposure to specified levels of radiation (under various bias conditions), the Vth of each MOS test sample was measured in situ. From these measurements, the changes in the Vth were plotted as a function of applied gate field and ionizing dose.

The test structures used in this work included small-scale-integration (SSI) circuits and discrete PMOS and NMOS devices. The SSI circuits were RCA-Z-CD4007AD (radiation hardened) and Fairchild F4007UB (nonradiation hardened) complementary MOS (PMOS) inverters. Both test structures, which were electrically identical, were composed of six enhancement-mode, aluminum gate transistors (three PMOS and three NMOS) on the same test chip. A primary difference between these two circuits was the radiation hardness level. The RCA chip was designed to tolerate 100 Krad(Si) of total ionizing radiation dose and remain within

specifications. The Fairchild chip was a "commercial grade" part with no designed radiation hardness. The discrete, nonradiation hardened PMOS and NMOS transistors were enhancement-type, Intersil 3N161 and 3N171 respectively. Each of these discrete part types was obtained from a single production run.

The test facility used in these proton irradiations was the Los Alamos National Laboratory's (LANL) Tandem Van de Graaff Accelerator. This accelerator was chosen because it could provide the desired energy of mono-energetic protons (10 MeV) at a continuous and very stable low beam current of 1 to 2 nA.

The proton irradiations were performed in a cryogenic evacuated test chamber which enclosed a rotating Faraday cup, a beam illuminator, two beam collimators, a rotating disk that holds the irradiated test samples, and a liquid nitrogen reservoir with a cold transfer finger. The Faraday cup (with a current integrator) was used to measure the proton beam current. Beam area and uniformity were defined, and held constant, by the collimators and the illuminator. These features, along with a remote-controlled beam-stop, allowed an accurate measurement of beam current, beam area, and beam exposure time. From these measurements and with the use of stopping power tables in Ref. 6, the proton fluence and the ionizing total dose for each irradiation were determined. Once the dose level was defined, a test sample affixed to the disk was rotated into the beam path and irradiated.

To irradiate a device at cryogenic temperatures, the cold finger from the liquid nitrogen reservoir (Fig. 1) was first brought into contact with the target cold sink on the disk, and the test sample was cooled to the required temperature. Note that the device temperature was monitored using a sensor on each of the test structures. When the proper temperature was reached, the proton beam was turned on and the desired dose was applied.

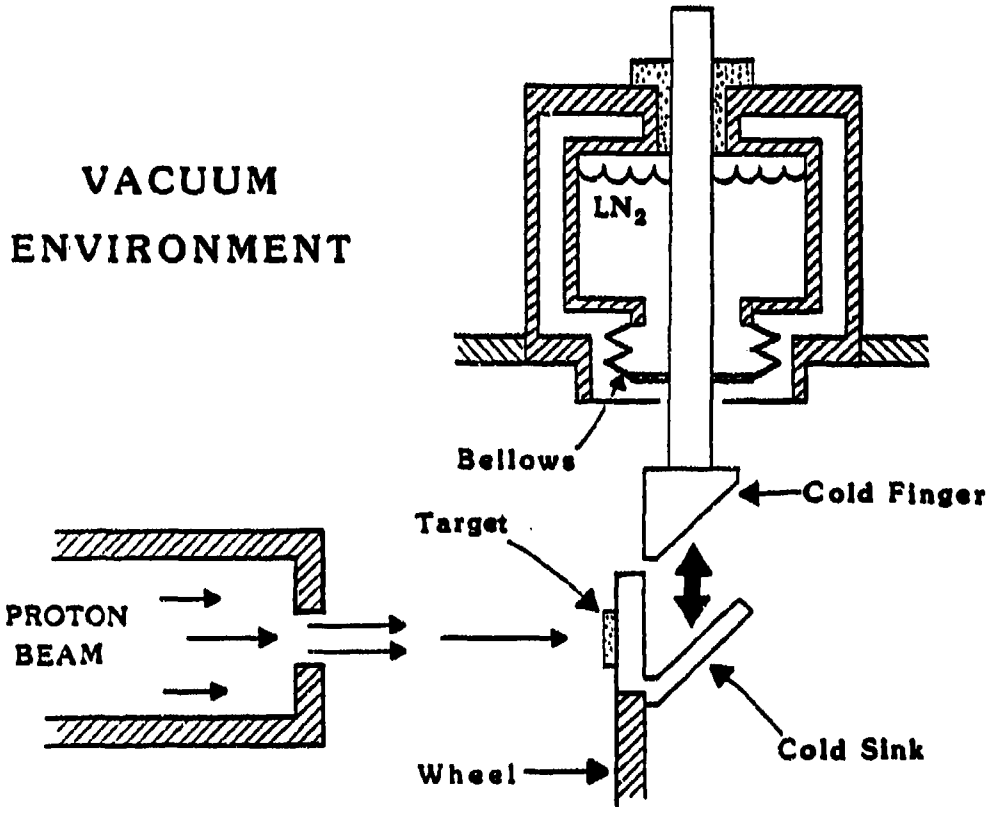


Figure 1. Cryogenic test setup for proton beam irradiations.

It is important when measuring the Vth of the MOS devices at cryogenic temperatures, that the test structures should not heat up during the measurement. If heating were to occur, rapid

annealing of the radiation damage would take place, and the true cold temperature damage responses would not be recorded. To avoid this heat-up factor, during a Vth measurement, a procedure different than that described in MIL-STD-750C (Method 3404) was used.

In this effort, Vth was measured by first applying a specified drain-to-source voltage (Vds), and then starting with a zero drain-to-source current (Ids), slowly applying a gate-to-source voltage (Vgs) until a small specified Ids was observed. At this point in the measurement, the Vgs was recorded and designated as Vth. The specified Ids for this recorded Vth, and for all of the test parts in this work was 1.0 μA. This low Ids value was chosen because it could be accurately measured with available test equipment, and it was not large enough to raise the temperature of the test structures during a Vth measurement.

A more detailed examination of this heat-up phenomena is presented in Section 4.0.

3.0 TEST RESULTS

Summaries of the test results are presented in Figs. 2 through 11. All of the plots illustrate the ionizing dose radiation damage from 10 MeV protons bombarding the selected MOS samples at 0 deg angle of incidence, while the samples were operating under various biases and temperatures. Specifically, in Figs. 2 through 9, the radiation damage is plotted as the change in the Vth (ΔVth) of the test devices, as a function of ionized dose in rad(Si). In Figs. 10 and 11, the damage is plotted as ΔVth versus Vgs for a total applied dose of 50 Krad(Si). In all of the plots, the radiation sample sizes ranged from 12 to 15 test transistors for each proton data bar.

Figures 2 and 3 show the radiation damage from 10 MeV protons bombarding the P-Channel cells on the radiation hardened RCA-Z CD4007AD test chips. The change in Vth versus ionized dose, when a Vgs of 0.0 V or -5.0 V was applied to the test cells operating at cold and room temperatures is plotted. Figure 2 presents the data for Vgs = 0.0 V, and Fig. 3 shows the data for Vgs = -5.0 V. The data in Fig. 2 show that the radiation damage produced in the PMOS devices was equal at both the cold and room temperatures. That is, after absorbing equal amounts of total dose (at the same rate), the changes in the Vth for the PMOS samples operating with zero gate biases were approximately equal. As an example, using ΔVth = -2.0 V as an arbitrary failure level, both temperature plots show that this occurred

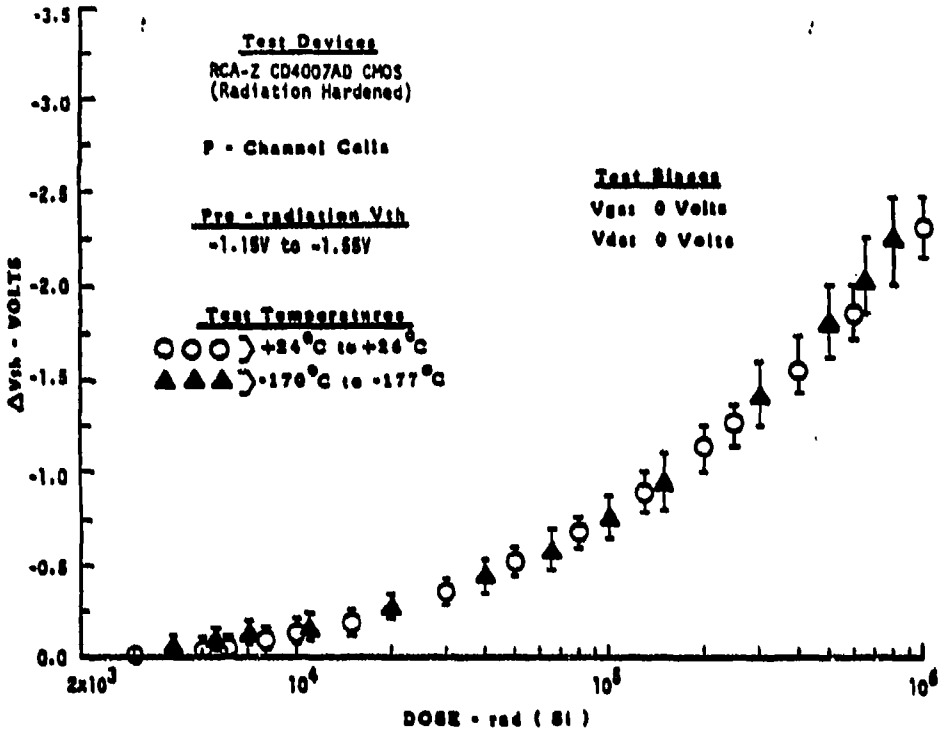


Figure 2. PMOS gate Vth shift versus 10 MeV proton dose for an applied Vgs of 0 V at cold and room temperatures.

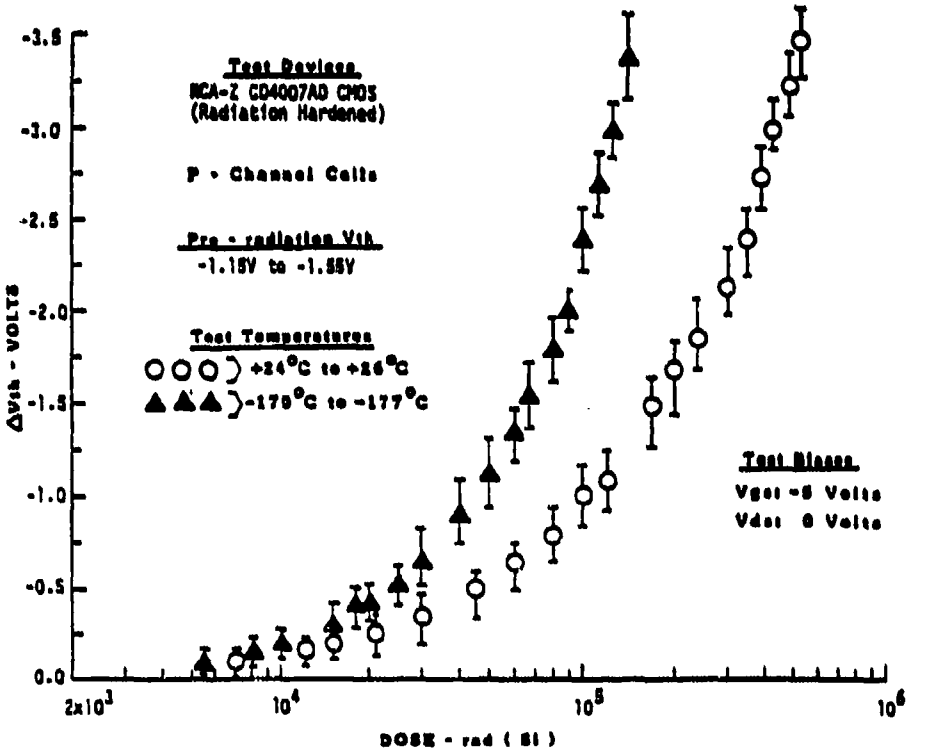


Figure 3. PMOS gate Vth shift versus 10 MeV proton dose for an applied Vgs of -5 V at cold and room temperatures.

after the test structures absorbed ≈700 Krad(Si). In Fig. 3, the data for the PMOS samples operating under a negative gate bias show that the permanent shift in the Vth was greater at cold temperatures than at room temperatures. At the cold temperature, the negatively biased devices required ≈90 Krad(Si) versus the 275 Krad(Si) at room temperatures to produce a ΔVth of -2.0 V.

The radiation effects from 10 MeV protons striking the N-Channel cells on the hardened RCA-Z CD4007AD devices are presented in Figs. 4 and 5. Figure 4 illustrates the ΔVth versus dose data for Vgs = 0 V, and Fig. 5 presents the ΔVth versus dose data for Vgs = +5 V. The data in both figures show that the application of a cold temperature has little effect on the radiation hardness of these samples. In fact, the plots showed that the cold temperature slightly enhanced the hardness level of the test devices. As an example, in Fig. 5, using ΔVth = -1.5 V as an arbitrary failure shift, the data bars showed that this occurred after absorbing ≈34 Krad(Si) of irradiation at room temperatures. At the tested cold temperature, an absorbed dose of ≈39 Krad(Si) was required to produced the same threshold shift. This was an increase of 5 Krad(Si) to produce the same ΔVth change.

Figures 6 and 7 present cold and room temperature results from 10 MeV protons irradiating the P-Channel cells on the non-radiation hardened Fairchild F4007UB circuits. The ΔVth versus ionizing dose for Vgs = 0 V is presented in Fig. 6, and the ΔVth

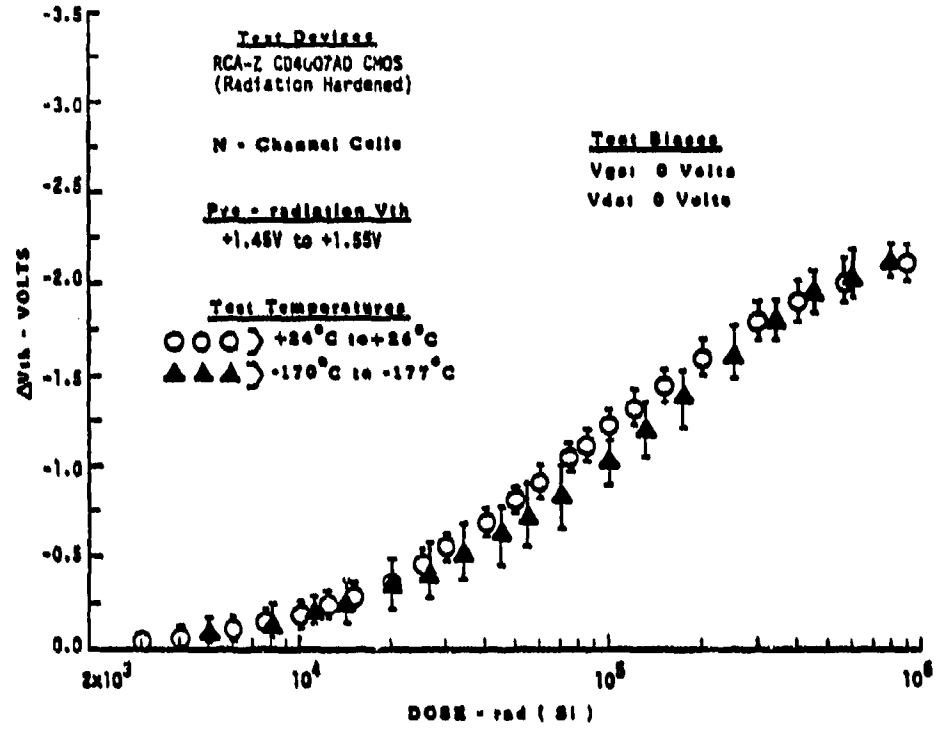


Figure 4. NMOS gate Vth shift versus 10 MeV proton dose for an applied Vgs of 0 V at cold and room temperatures.

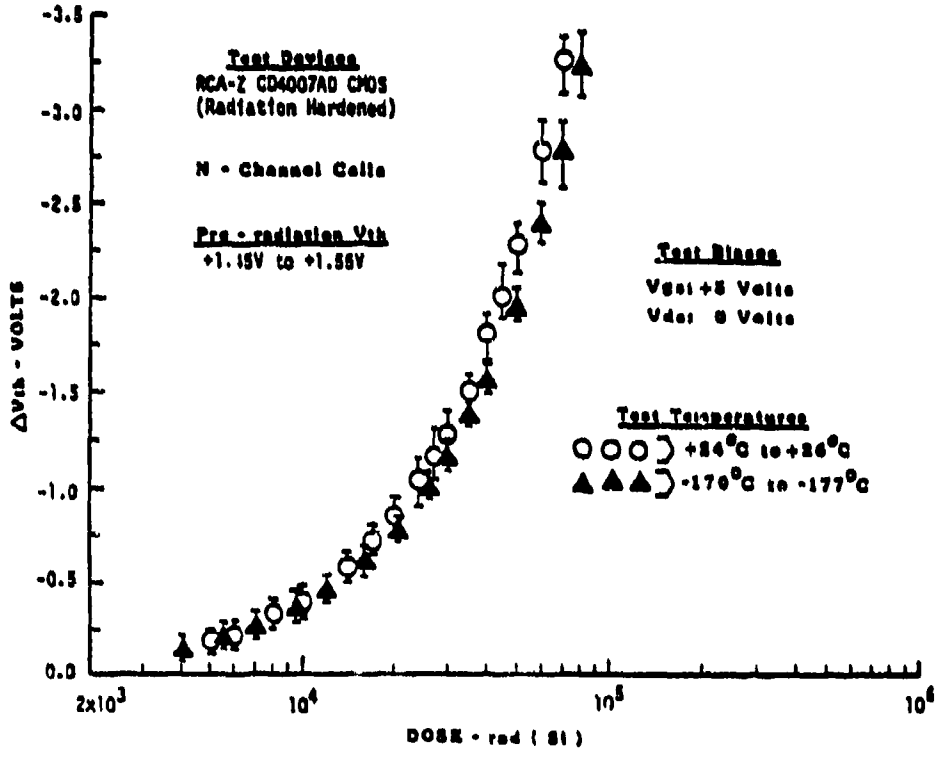


Figure 5. NMOS gate Vth shift versus 10 MeV proton dose for an applied Vgs of +5 V at cold and room temperatures.

versus ionizing dose for Vgs = -5 V is plotted in Fig. 7. Both series of plots show that the radiation damage versus dose was greater at cold temperatures than at room temperatures. Again, using a ΔVth = -2.0 V as an arbitrary failure shift for the PMOS cells, Fig. 6 shows that at the cold temperatures, the zero biased samples needed ≈180 Krad(Si) of total dose to produce this shift, whereas, in the room temperatures tests, ≈250 Krad(Si) was required to produced the same results. In the negatively biased plots (Fig. 7), ≈40 Krad(Si) was needed at the cold temperatures to produce the -2.0 V shift. Approximately 74 Krad(Si) was required at room temperatures.

The effects on the Fairchild F4007UB N-Channel cells from the bombarding protons are presented in Figs. 8 and 9. Figure 8 shows the cold and room temperature data for Vgs = 0 V, and Fig. 9 illustrates the cold and room temperature plots for Vgs = +5 V. The data in Fig. 8 show that the radiation damage produced in the zero biased NMOS cells was unaffected by the change in the temperature. That is, ΔVth versus dose was equal at both test temperatures. However, in Fig. 9, the positively biased devices were affected by temperature change. At the cold temperatures, the radiation damage was less than the damage produced at room temperatures. Using a ΔVth = -2.25 V as the arbitrary failure criteria, the room temperature test showed that this Vth shift occurred after absorbing ≈45 Krad(Si). In the cold temperature evaluations, an additional dose of 15 Krad(Si), or a total 60 Krad(Si), was needed to produce the same Vth change.

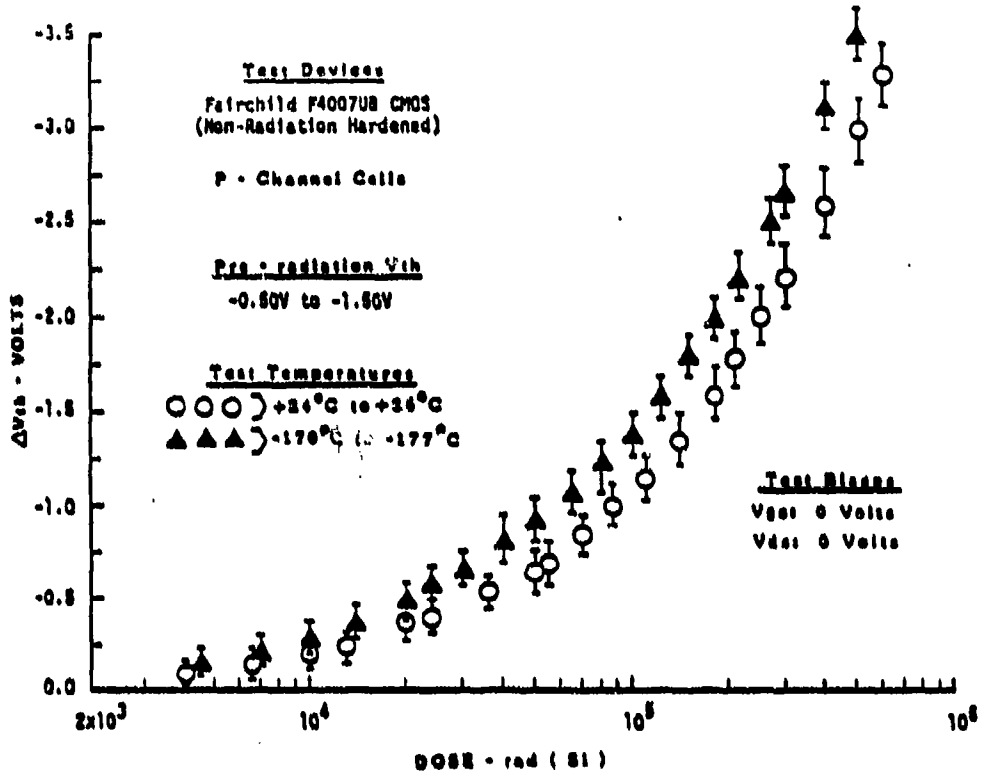


Figure 6. PMOS gate Vth shift versus 10 MeV proton dose for an applied Vgs of 0 V at cold and room temperatures.

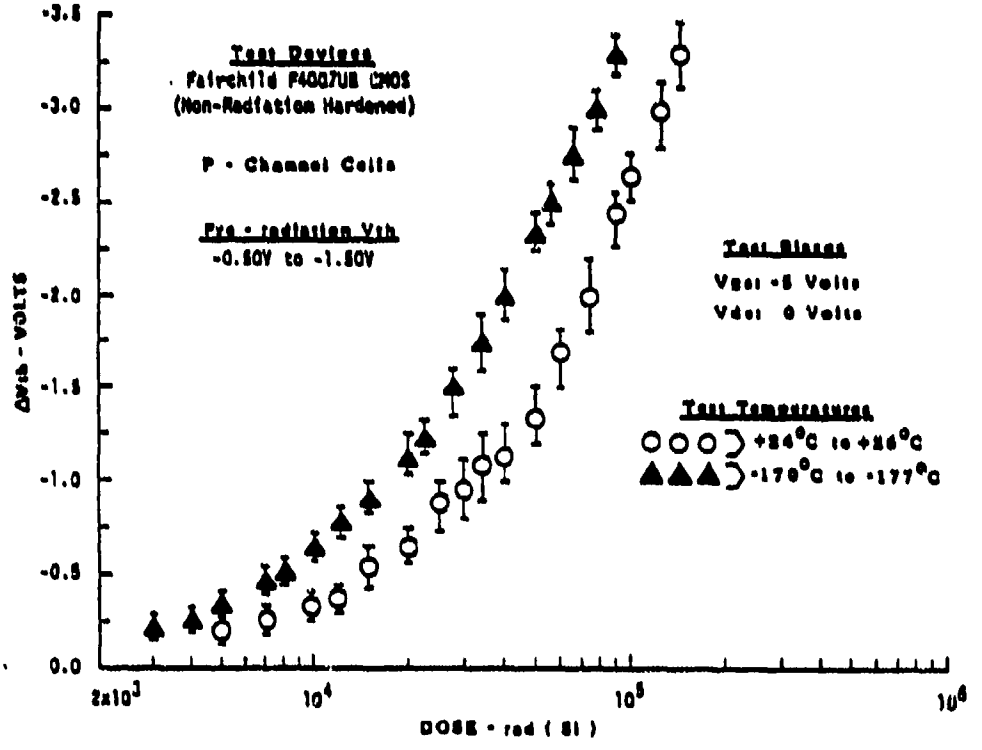


Figure 7. PMOS gate Vth shift versus 10 MeV proton dose for an applied Vgs of -5 V at cold and room temperatures.

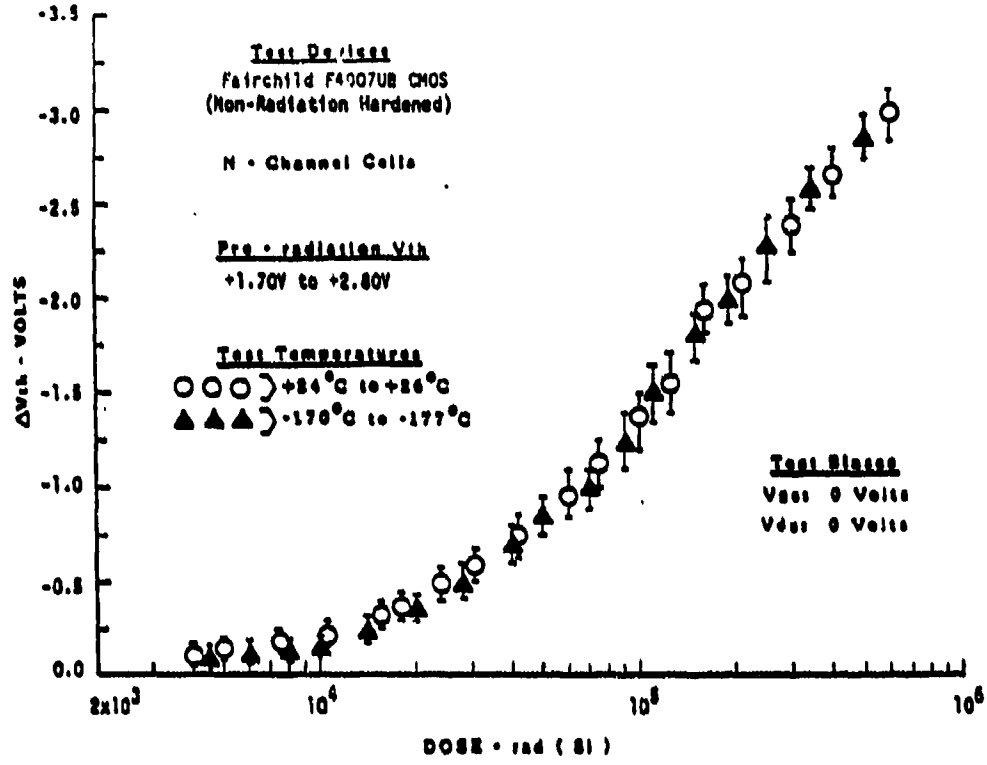


Figure 8. NMOS gate Vth shift versus 10 MeV proton dose for an applied Vgs of 0 V at cold and room temperatures.

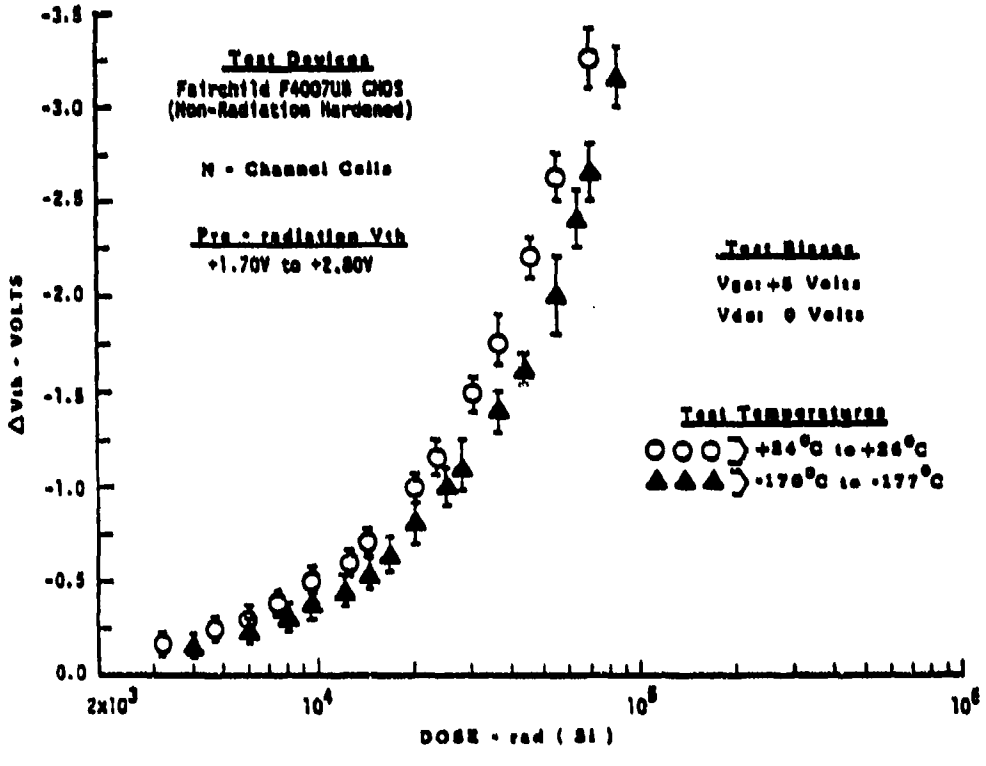


Figure 9. NMOS gate Vth shift versus 10 MeV proton dose for an applied Vgs of +5 V at cold and room temperatures.

Figure 10 presents the cold and room temperature irradiations on the discrete, diode protected gate, Intersil 3N161 PMOS silicon transistors. The ΔVth shifts versus Vgs are plotted at two temperatures for an applied 10 MeV proton dose of 50 Krad(Si). The plots in this figure show that the radiation damage was proportional to the applied negative Vgs and inversely proportional to device's temperature. That is, as the magnitude of -Vgs was increased, the change in Vth was greater at the cryogenic temperatures than at the room temperatures. As an example, with a Vgs = -10 V, the ΔVth at room temperature was ≈-4.8 V. For the same Vgs at the tested cold temperatures, the ΔVth was -5.6 V. This was an increase/change of -0.8 V.

The radiation effects from 10 MeV protons bombarding the discrete (nondiode protected) Intersil NMOS silicon transistors are presented in Fig. 11. The ΔVth versus Vgs for an applied proton dose of 50 Krad(Si) is shown at cold and room temperatures. Note that since there is no gate protection on this device type, tests were performed both with a positive and a negative voltage across the gate-to-source terminals. Results from these tests showed that the radiation damage was greater at room temperatures than at cryogenic temperatures for a positively biased Vgs. However, operating under a negatively biased Vgs, the results were reversed. The damage was greater at the cold temperatures than at the room temperatures.

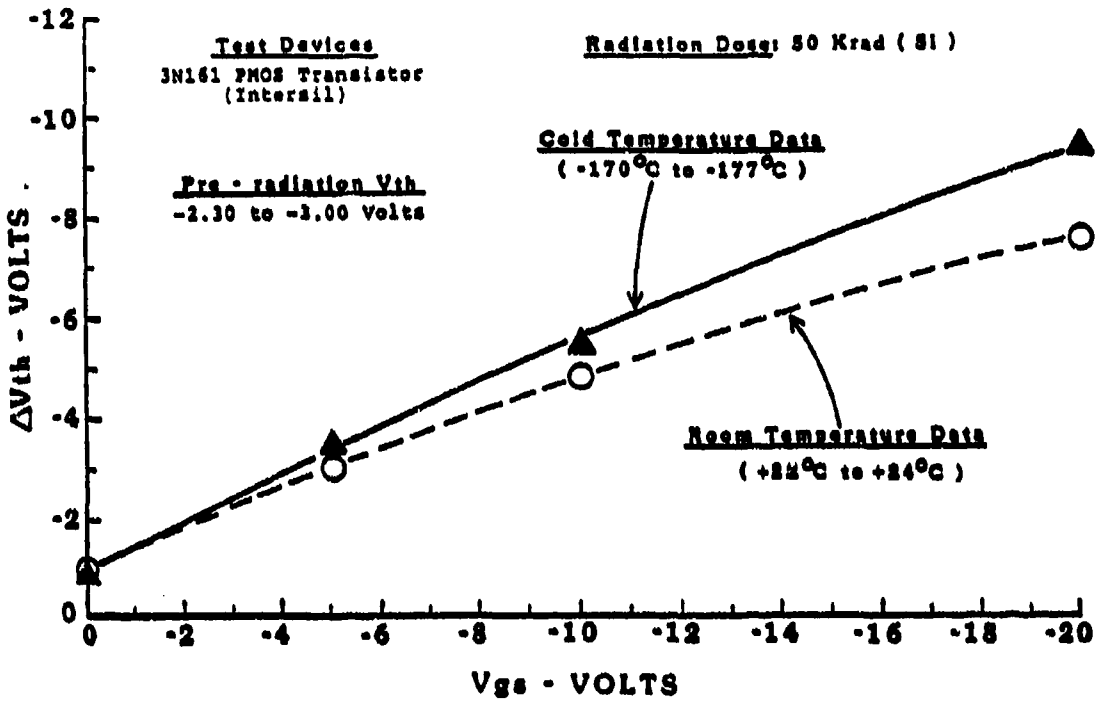


Figure 10. PMOS gate Vth shift versus Vgs for a 10 MeV proton dose of 50 Krad (Si) at cold and room temperatures.

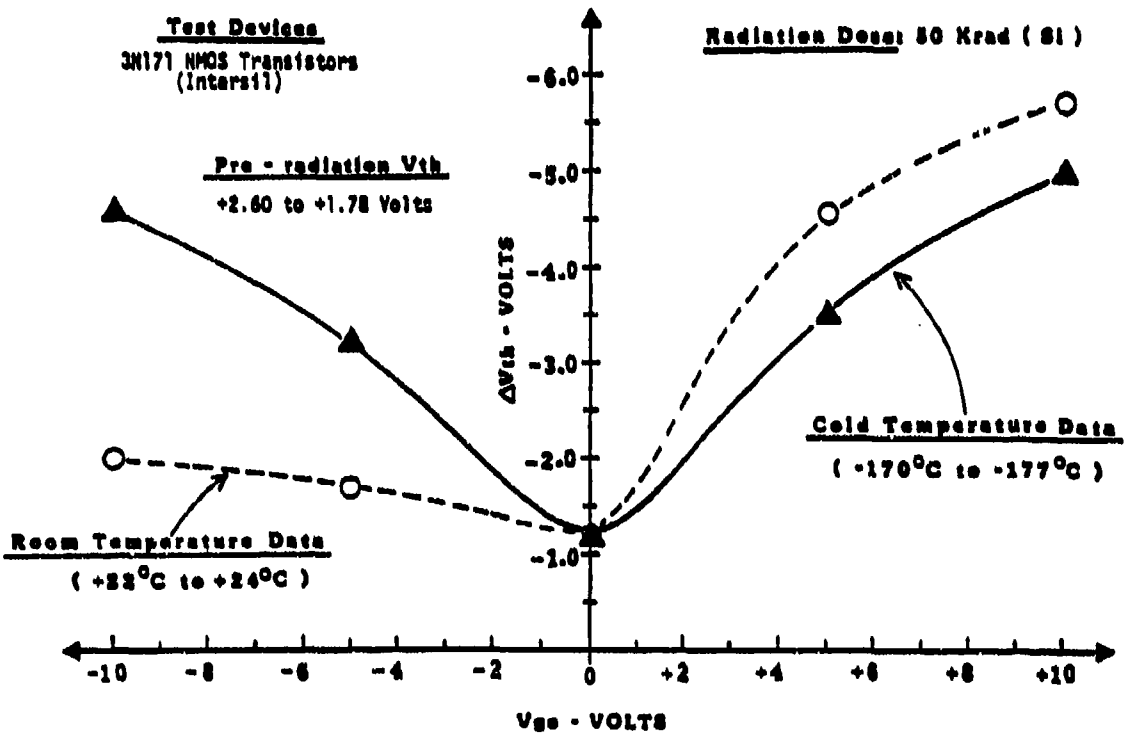


Figure 11. NMOS gate Vth shift versus Vgs for a 10 MeV proton dose of 50 Krad (Si) at cold and room temperatures.

4.0 DISCUSSION

The results presented in this report show the radiation damage mechanism for high energy 10 MeV protons striking cryogenically operated MOS type electronics are similar (in certain aspects), to that observed in Co^{60} and energetic electrons irradiations. That is, at the cold temperatures tested, some of the test samples (the PMOS transistors or the test devices irradiated under a negative Vgs), suffered greater radiation damage per dose than for similar irradiations at room temperatures (Figs. 3, 6, 7, 10 and 11). These results support the cold-temperature model presented in Section 1.0.

In contrast, the results from the NMOS test samples (the test devices irradiated under a positive Vgs) did not explicitly support this cryogenic model. The reason was the NMOS devices irradiated at cold temperatures under a positive Vgs, suffered less (or equivalent) damage per dose than similar irradiations at room temperatures (Figs. 5, 9 and 11). To fully satisfy the model, the radiation damage in the biased NMOS devices should have been greater at the cold temperatures than at the room temperatures. This should have been especially true for the RCA radiation-hardened MOS structures. There are several possibilities for this disparity. A few are: variations in the test samples used in this work versus the test devices used in other efforts, differences in the cryogenic test temperatures, and dissimilarities in the damage mechanisms between the protons and the Co^{60} gamma rays (or high energy electrons).

The most plausible explanation for the disparities is the differences in the selected test samples. Most of the devices used in this work were commercial grade chips, with no radiation hardness. The only chip type that was built with a "firm" tolerance to radiation was the RCA-Z CD4007AD, and the hardness level of this chip was only designed for 100 Krad(Si). However, test samples used in the other efforts (Refs. 2 through 5) were specially built and had greater tolerance to ionising radiation. Many of the special devices, at room temperatures, had a hardness level beyond 1.0 Mrad(Si). These high levels of radiation hardness translated into small Vth changes in room temperature irradiations and larger Vth changes (because of large numbers of holes frozen in the gate oxides) in cold temperature irradiations. It is highly probable that if the hardness level of the RCA chip was increased to 1.0 Mrad(Si), the positive gate-biased NMOS cells would suffer a greater damage from ionized radiation at cold temperatures than at room temperatures.

Another parameter that may have been a factor in these results was temperature. In this effort (because of limitations in the test fixtures) the coldest temperature used was between -170°C and -177°C. In the work performed for the references, the test temperatures were close to that of liquid nitrogen (-197°C). This translates into a temperature differential of -20°C to -27°C between the reference data and the work performed in this effort. Since the cold temperature model was mainly proposed

for temperatures at (or very near) -197°C, the NMOS devices irradiated in this work may not have generated as large a frozen-in hole population within the oxides as samples bombarded at -197°C. This could add to the explanation of why the radiation damage in the positively biased NMOS devices evaluated in this work was less than the damage produced at room temperatures.

A third factor that could explain the unexpected NMOS results was a possible difference in the damage mechanism between the 10 MeV protons and the Co^{60} gamma rays (or high energy electrons). In high energy proton irradiations, the generation of electron-hole pairs in the gate oxides of the test samples are localized around the tracks of the incident protons. For Co^{60} and high energy electron exposures, the ionization regions are generated in an isotropic manner throughout the oxides. This difference in the way the created electrons and holes are dispersed may alter the distribution of the frozen-in holes within the oxides. In the proposed cryogenic model, it was assumed that the immobile holes produced a uniform positive charge density throughout the gate oxides. If the dense ionization tracks produced by the protons resulted in a different charge distribution, then the model may not always apply to protons. Countering this hypothesis were the results from the biased PMOS irradiations, which showed that the proton damage did correlate with the model predictions. To get a better answer on this possible factor, cold-temperature Co^{60} irradiations would have to be performed on the same test sample types that were

evaluated in the 10 MeV protons. From such tests, true comparisons between the protons and Co^{60} gammas can be made, and the differences in the damage mechanisms (if any) can better be determined. Such correlation tests are planned in the near future.

Finally, as noted in Section 2.0, if the test devices (operating at cryogenic temperatures) were allowed to increase significantly in temperature during a Vth measurement, the correct cold temperature responses would not be recorded. This would be true in this work, if the procedures outlined in MIL-STD-750 (Method 3404) were used for measuring Vth. The MIL-STD-750 calls for measuring the gate Vth of a MOS transistor by a procedure called the Saturated Threshold Voltage Method. This method measures the gate Vth while the MOS device is operating in the Saturation Region (the region of operation between the Linear and the Breakdown modes) of the device. In practice, the Saturation Region represents the normal operating region of a MOS transistor.

Figure 12 illustrates this MIL-STD procedure for measuring the Vth of a PMOS device. The Vgs versus the square-root of the drain current minus the drain leakage current is presented. The Vth is obtained by first measuring the drain-source current at several values of Vgs for a fixed Vds (-10 V). Then on a linear scale, the square root of the difference of the drain current and the leakage current is plotted as a function of Vgs. This measurement is repeated until Vgs = Vds, or the maximum drain

current is reached. Next, the maximum tangent to the resulting curve is extrapolated downward to the Vgs axis. The resulting intersection of this line with the Vgs axis is the measured Vth.

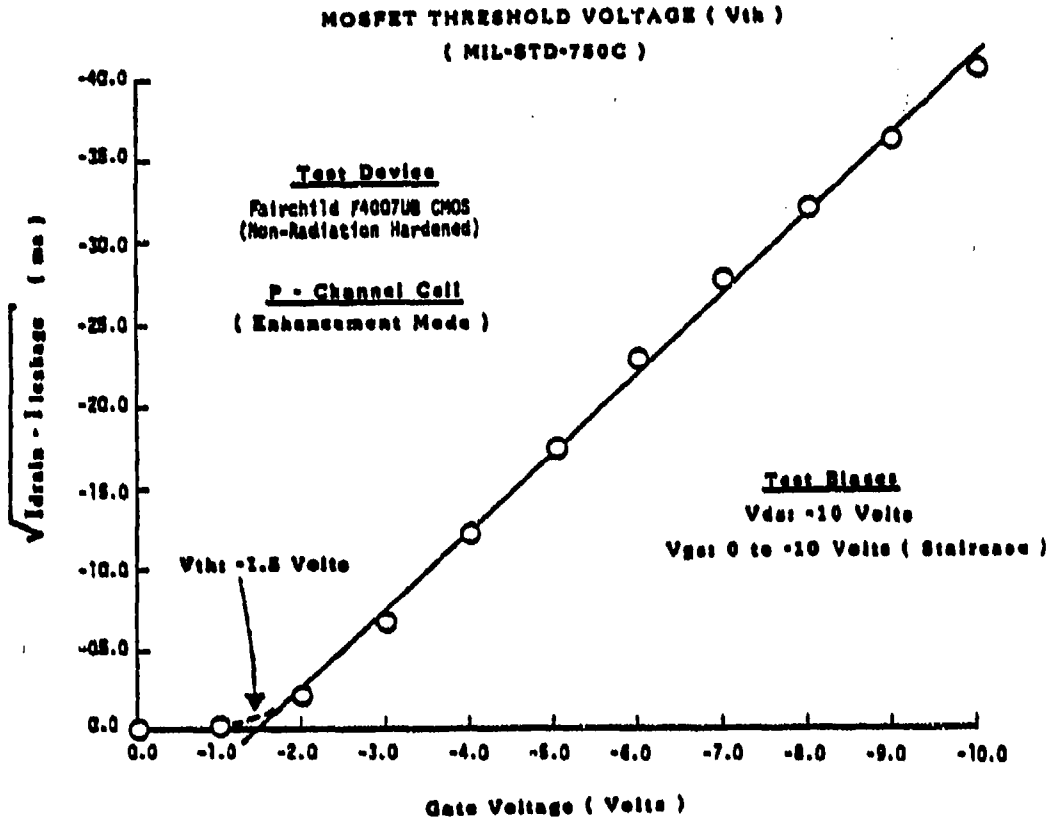


Figure 12. Gate to source voltage versus the square-root drain current minus leakage current for a P-Channel enhancement mode MOSFET using the Saturated Threshold Voltage Method.

This procedure has one major drawback: it heats the test device during the measurement. In early tests in this effort, Vth measurements were made with the aid of a computer using this technique. A sample of the results is presented in Fig. 13.

The Vth shift versus 10 MeV protons for Vgs = +5 V recorded at cold and room temperatures is plotted in Fig. 13. The devices were N-Channel cells on the RCA-Z CD4007AD test chips, picked

from the same lot that was evaluated in Fig. 5 using the low Ids method. The results in Fig. 13 show abrupt recoveries in the ΔVth for the samples irradiated at the cold temperatures. This sudden annealing in the ΔVth during the cold temperature irradiations was observed in all of the test devices measured by the MIL-STD-750 method.

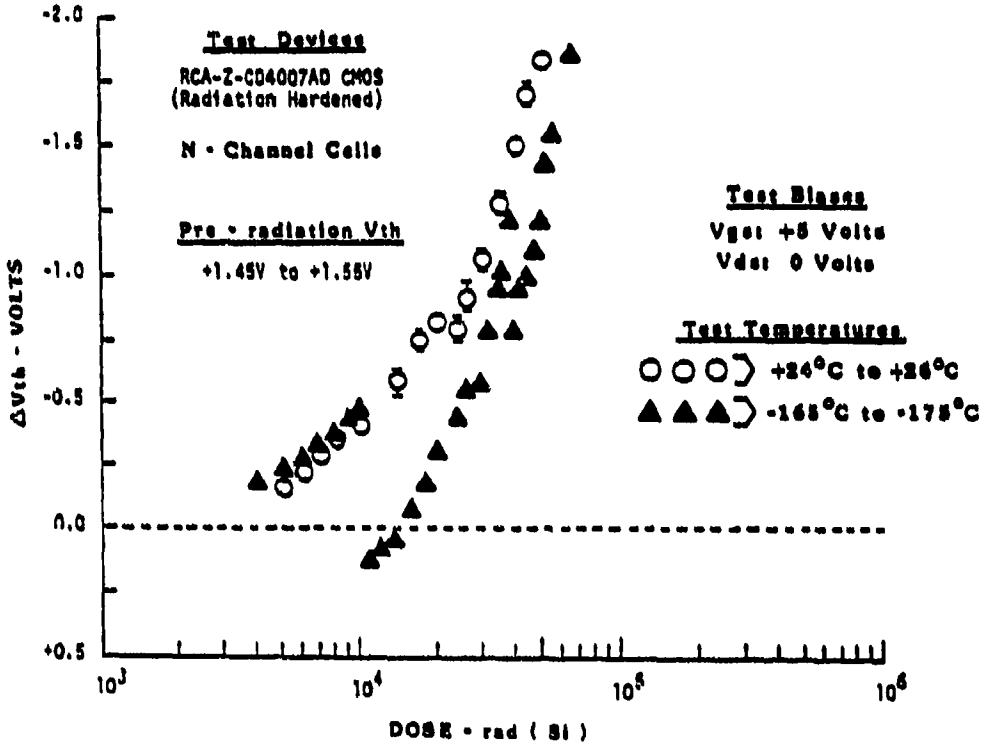


Figure 13. NMOS gate Vth shift versus 10 MeV proton dose for an applied Vgs of +5 V at cold and room temperatures measured by the MIL-STD-750 method.

The cause of these sudden recoveries in the Vth was attributed to the MIL-STD procedure heating the test devices during the measurements. This Vth measuring technique causes high currents to be generated in the drain-source channels, especially when the Vgs is allowed to increase in value and approach the value of the Vds. It was concluded that these high drain-source currents were the cause of this heat-up factor. Tests were

performed, and it was discovered that the MIL-STD-750C method was raising the temperature of the test structures (for a few seconds) from $\approx$-170°C to $\approx$-104°C. It was also determined that this short heat-up pèriod was enough to cause the mobility of the frozen-in holes (within the gate oxides) to suddenly increase and to cause them to recombine with electrons injected from the conducting drain-source channels. Note that these high channel currents increased the probability of thermal breakdowns in the barriers between the gate-oxides and the silicon channels, thereby increasing the chances of injection currents.

To counter this heat-up factor a Vth measurement procedure which ensured that the test structures would not change temperature during the cryogenic measurements had to be employed. Since, at the time of this work, there was no known standard available for measuring Vth at cold temperatures, a method was devised (with the agreement of all the parties involved). The chosen method was to measure a Vth that would generate a small, specified (but measurable) Ids. The important parameter that had to be determined was ΔVth versus dose. It was felt that as long as the Vth was measured with consistency (using the same low Ids for each measurement), the ΔVth versus dose would be a true measurement of the proton damage. This low Ids method is outlined in Section 2.0.

5.0 CONCLUSION

The primary ionizing radiation damage mechanism from 10 MeV protons bombarding cryogenically operated biased MOS type electronics is like that of Co^{60} gamma rays and high energy electrons. That is, at cold temperatures (close to that of liquid nitrogen), large numbers of radiation induced holes generated in a biased gate oxide of a MOS device become immobile and are trapped in the oxide, somewhere between the gate and channel interfaces. This phenomenon results in a large hole population, that has escaped recombination and is distributed throughout the oxide. The result is that for equal amounts of total ionizing dose absorbed, the radiation damage produced in biased MOS structures at cold temperatures is not equivalent to similar irradiations at room temperatures.

Specifically, for MOS devices (P-Channel or N-Channel) bombarded by 10 MeV protons, under applied negative gate biases, the radiation damage per dose absorbed would be greater at cold temperatures than at room temperatures. This would be true for both radiation hardened and nonradiation hardened MOS structures. This will not be true for MOS devices operating under positive gate biases. Nonradiation hardened MOS transistors, bombarded by 10 MeV protons, operating under positive gate bias conditions, will suffer less radiation damage per dose at cold temperatures than at room temperatures.

Depending upon the hardness level, positively biased MOS devices that are classified as radiation hardened, may or may not suffer

greater proton damage per dose at cold temperatures than at room temperatures. The harder the device is to ionizing radiation at room temperatures, the higher the probability the structure will suffer greater radiation damage at cold temperatures.

Finally, if the irradiated cold temperature MOS devices were allowed to heat to $\approx -123^{\circ}C$ or warmer, the proton induced trapped holes would suddenly become mobile, and the radiation damage within the oxides would anneal rapidly.

REFERENCES

1. Nielsen, R.L., and Nichols, D.K., "Total Dose Effects of Ionizing Radiation on MOS Structures at 90 K," IEEE Transactions on Nuclear Science, Vol. NS-20, No. 6, December 1973.

2. Sander, H.H., and Gregory, B.L., "Unified Model of Damage Annealing in CMOS, from Freeze-In to Transient Annealing," IEEE Transactions on Nuclear Science, Vol. NS-22, No. 6, December 1975.

3. Srour, J.R., et al., "Radiation-Induced Charge Transport and Charge Buildup in SiO Films at Low Temperatures," IEEE Transactions on Nuclear Science, Vol. NS-23, No. 6, December 1976.

4. Boesch, H.E., and McGarrity, J.M., "Charge Yield and Dose Effects in MOS Capacitors at 80 K," IEEE Transactions on Nuclear Science, Vol. NS-23, No. 6, December 1976.

5. Srour, J.R., and Chiu, K.Y., "MOS Hardening Approaches for Low-Temperature Appications," IEEE Transactions on Nuclear Science, Vol. NS-24, No. 6, December 1976.

6. Janni, J.F., Atomic Data and Nuclear Data Tables, Academic Press. New York, NY, Vol. 27, Nos. 4/5, July/September 1982.